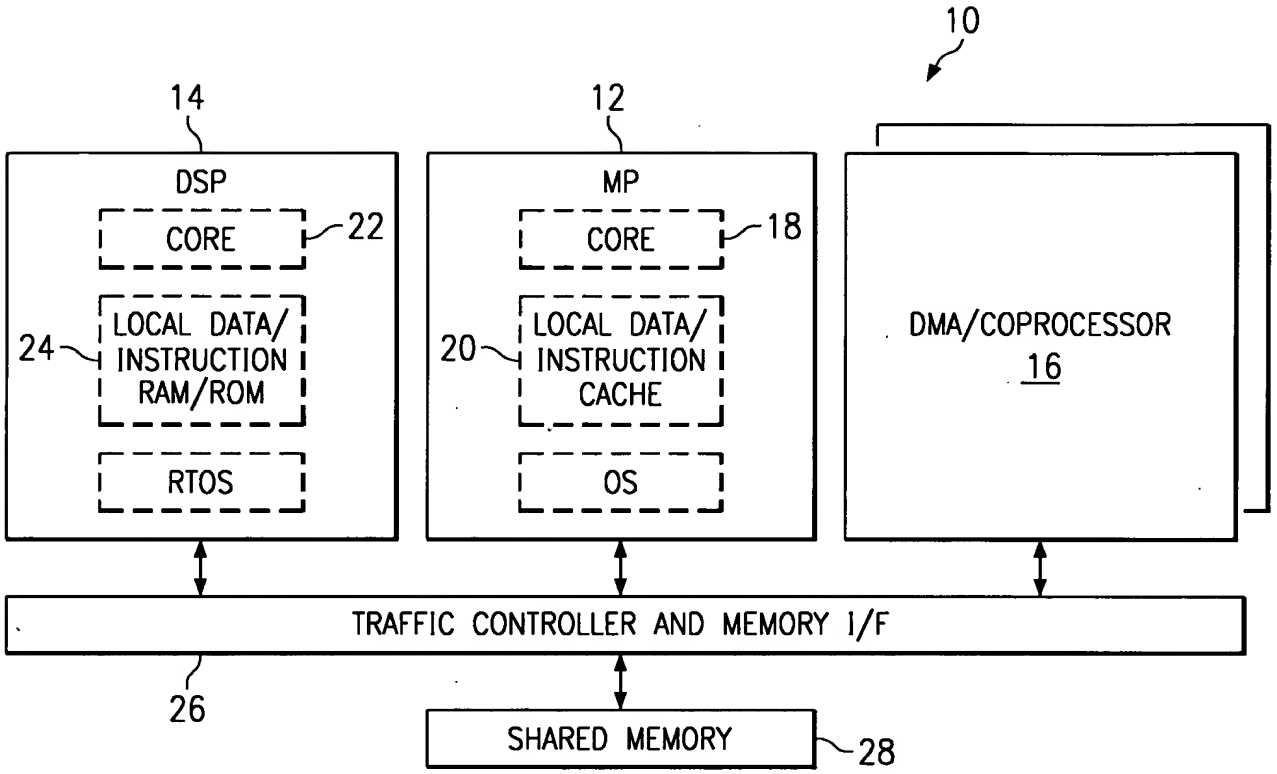
10
14
12
DSP
CORE
22
LOCAL DATA/
INSTRUCTION
RAM/ROM
24
RTOS
MP
CORE
18
LOCAL DATA/
INSTRUCTION
CACHE
20
OS
DMA/COPROCESSOR
16
TRAFFIC CONTROLLER AND MEMORY I/F
26
SHARED MEMORY
28

FIG. 1

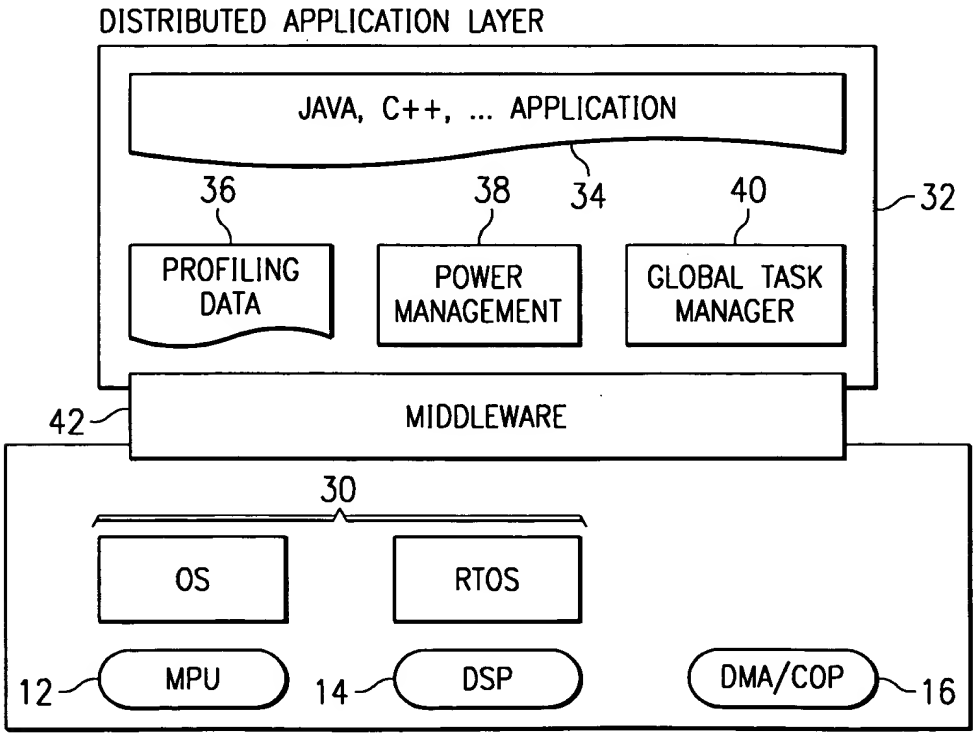
DISTRIBUTED APPLICATION LAYER
JAVA, C++, ... APPLICATION
34
36
38
40
32
PROFILING
DATA
POWER
MANAGEMENT
GLOBAL TASK
MANAGER
42
MIDDLEWARE
30
OS
RTOS
12
MPU
14
DSP
DMA/COP
16

FIG. 2

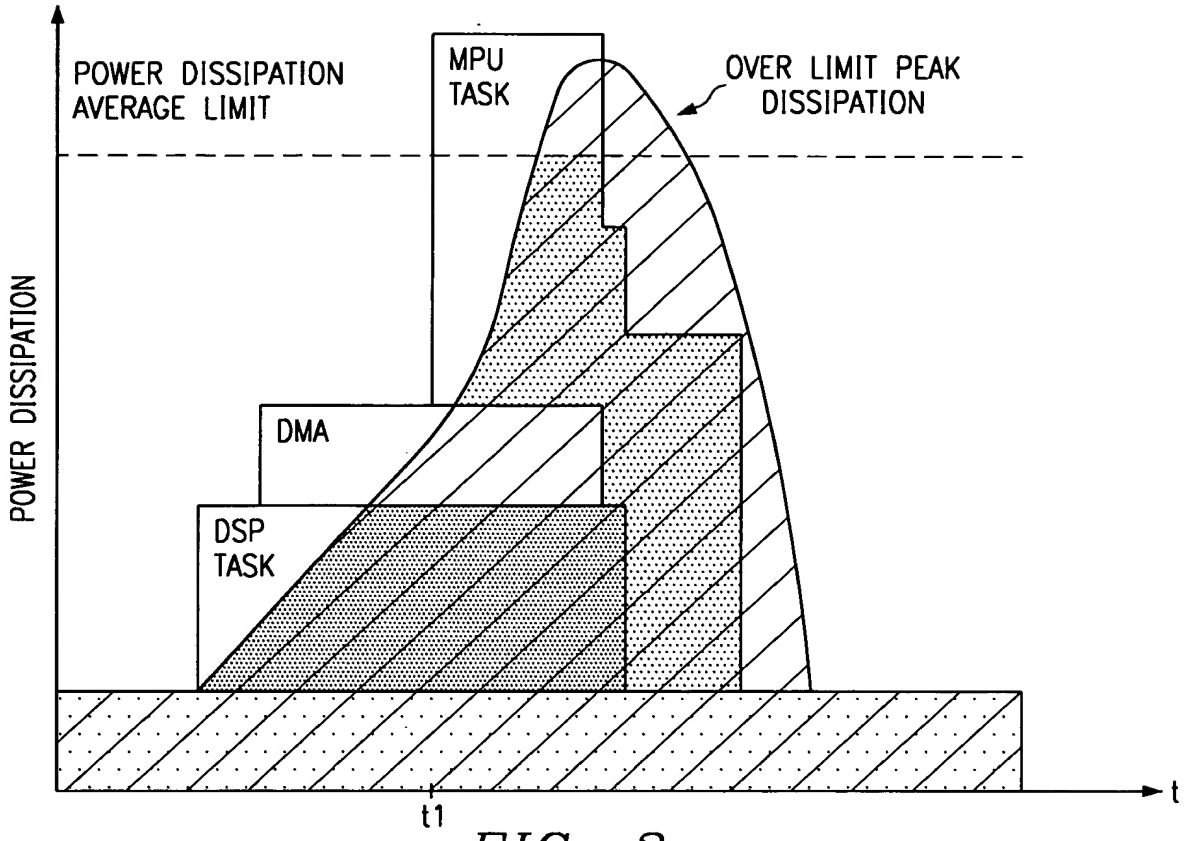
POWER DISSIPATION
AVERAGE LIMIT
MPU
TASK
OVER LIMIT PEAK
DISSIPATION
POWER DISSIPATION
DMA
DSP
TASK
t1
t

FIG. 3a

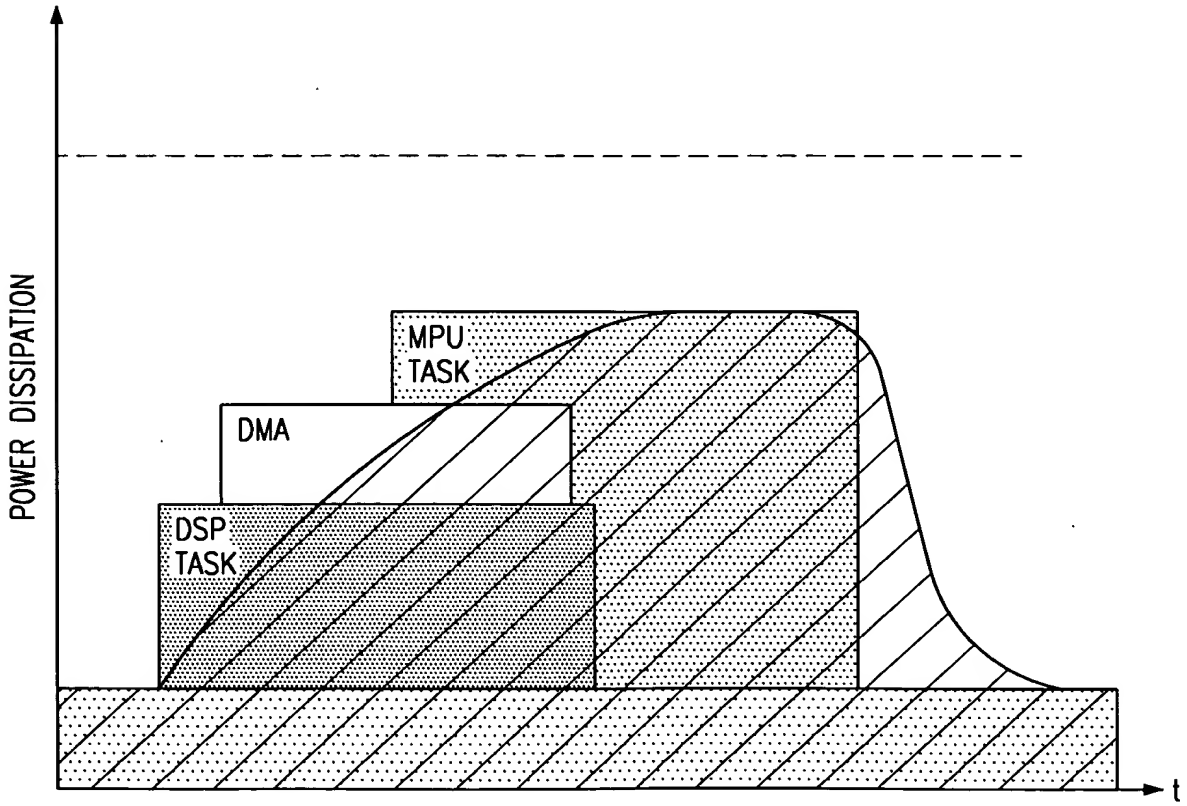
POWER DISSIPATION
MPU
TASK
DMA
DSP
TASK
t

FIG. 3b

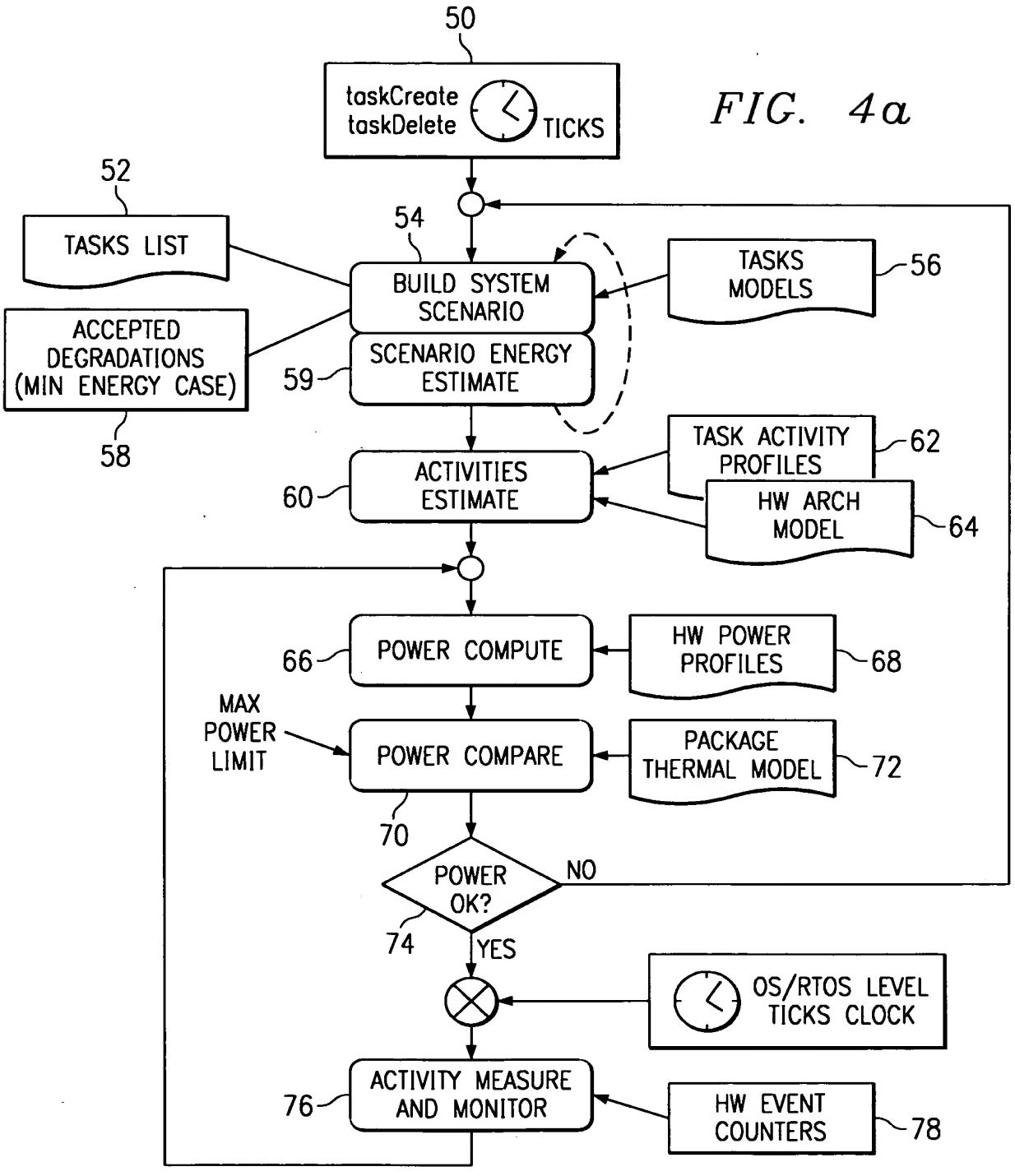
50
taskCreate
taskDelete
TICKS
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
58
59
SCENARIO ENERGY ESTIMATE
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4a

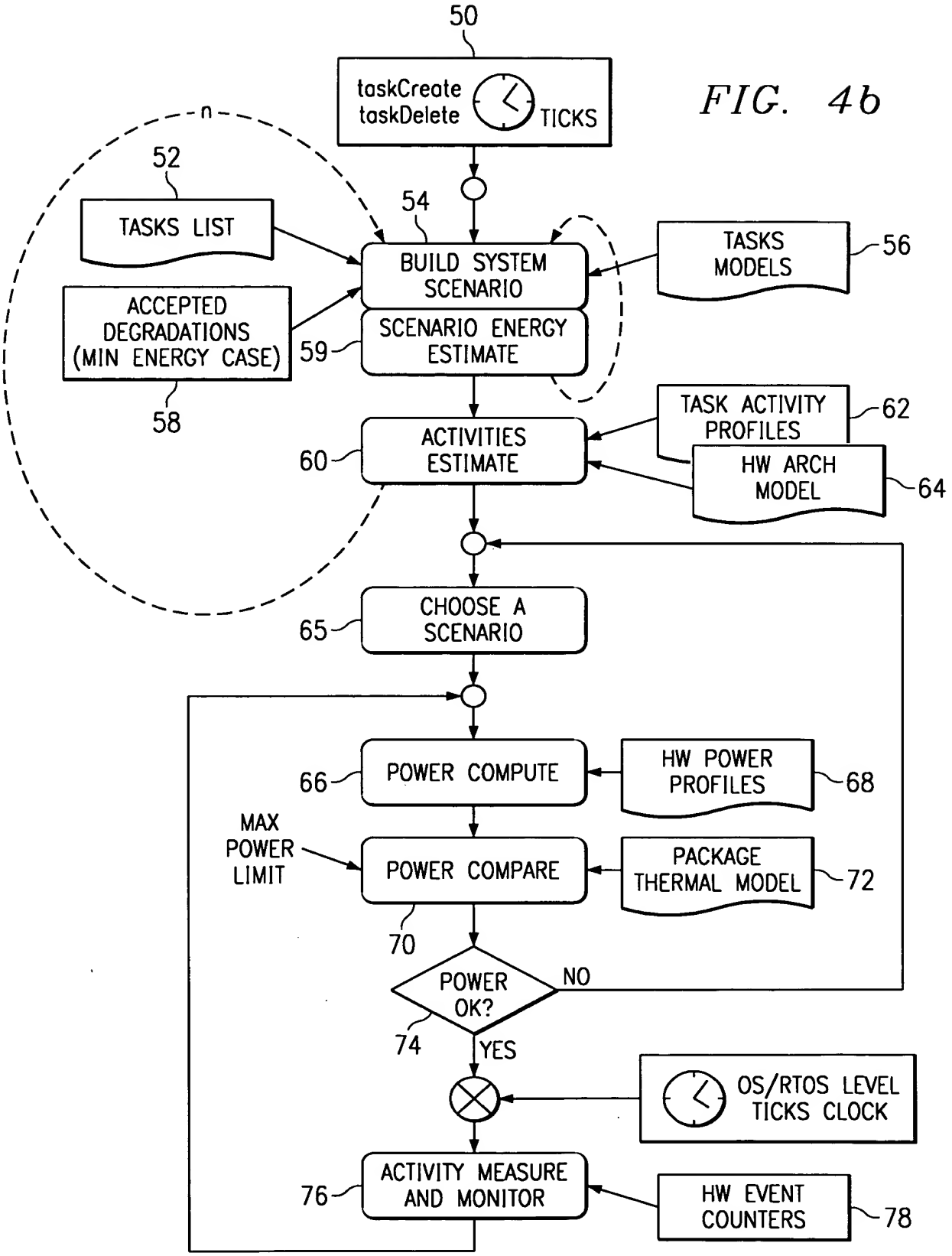
50
taskCreate
taskDelete
TICKS
n
52
TASKS LIST
54
BUILD SYSTEM SCENARIO
TASKS MODELS
56
ACCEPTED DEGRADATIONS (MIN ENERGY CASE)
59
SCENARIO ENERGY ESTIMATE
58
TASK ACTIVITY PROFILES
62
60
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
65
CHOOSE A SCENARIO
66
POWER COMPUTE
HW POWER PROFILES
68
MAX POWER LIMIT
POWER COMPARE
PACKAGE THERMAL MODEL
72
70
POWER OK?
NO
74
YES
OS/RTOS LEVEL TICKS CLOCK
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78

FIG. 4b

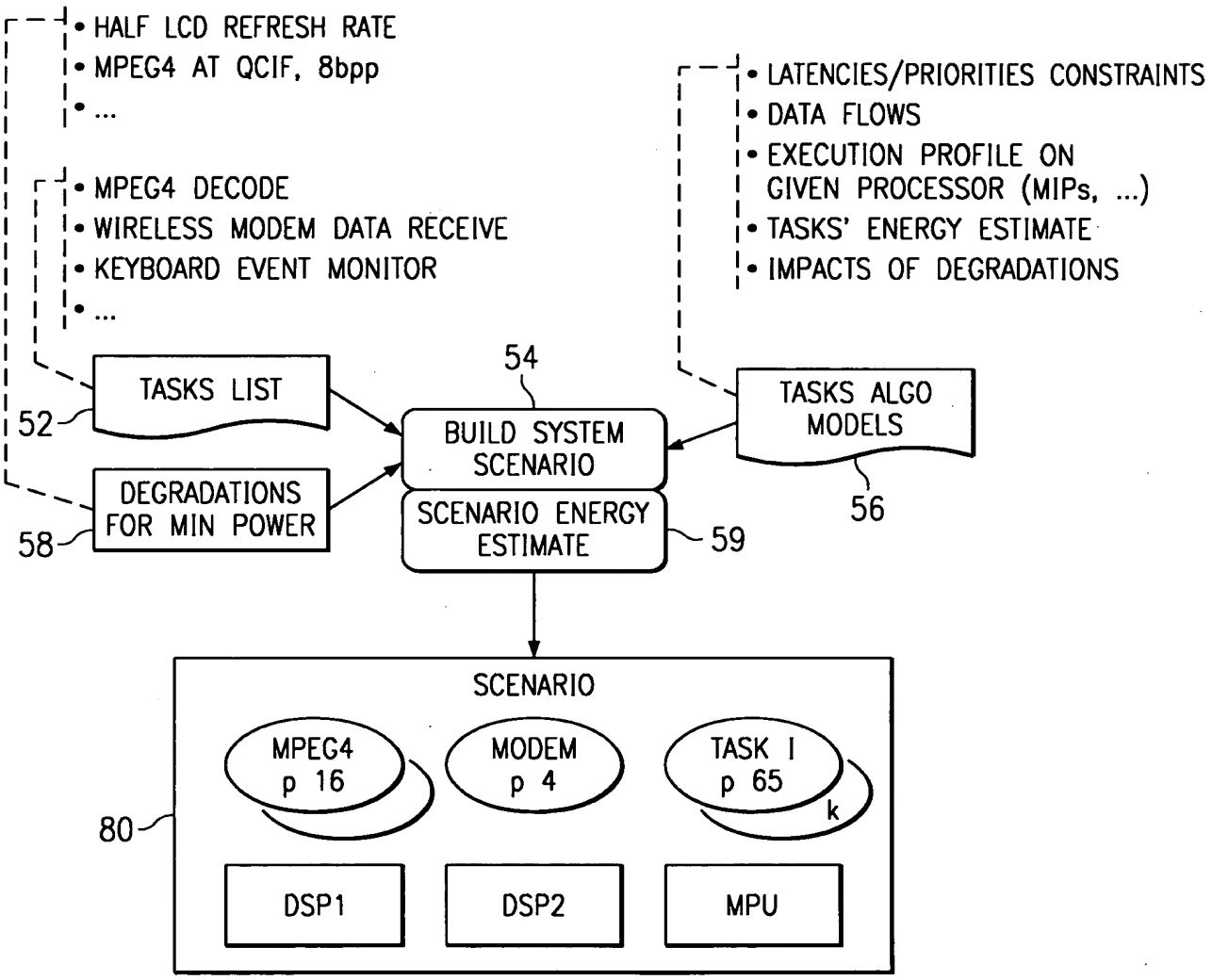
• HALF LCD REFRESH RATE
• MPEG4 AT QCIF, 8bpp
• ...
• MPEG4 DECODE
• WIRELESS MODEM DATA RECEIVE
• KEYBOARD EVENT MONITOR
• ...
• LATENCIES/PRIORITIES CONSTRAINTS
• DATA FLOWS
• EXECUTION PROFILE ON GIVEN PROCESSOR (MIPs, ...)
• TASKS' ENERGY ESTIMATE
• IMPACTS OF DEGRADATIONS
TASKS LIST
52
DEGRADATIONS FOR MIN POWER
58
54
BUILD SYSTEM SCENARIO
SCENARIO ENERGY ESTIMATE
59
TASKS ALGO MODELS
56
SCENARIO
MPEG4 p 16
MODEM p 4
TASK I p 65
k
80
DSP1
DSP2
MPU

FIG. 5

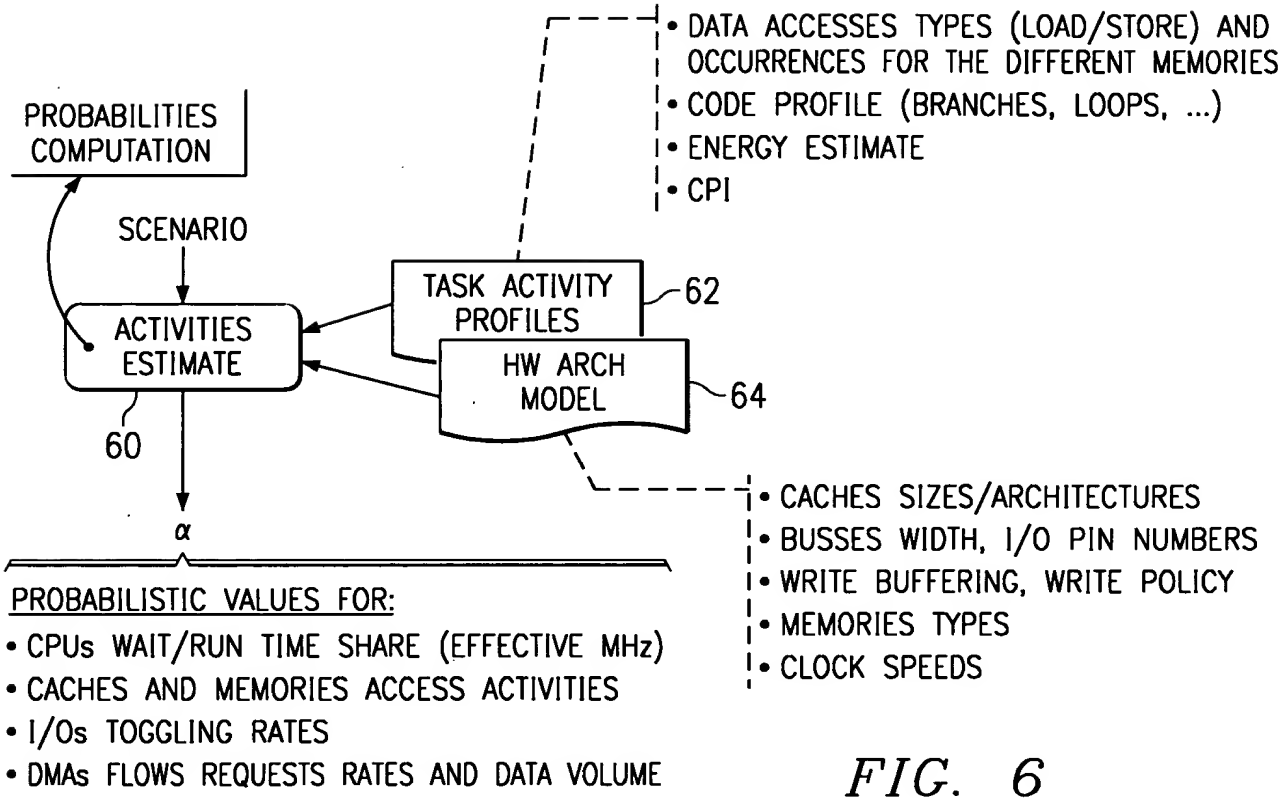
• DATA ACCESSES TYPES (LOAD/STORE) AND OCCURRENCES FOR THE DIFFERENT MEMORIES
• CODE PROFILE (BRANCHES, LOOPS, ...)
• ENERGY ESTIMATE
• CPI
PROBABILITIES COMPUTATION
SCENARIO
TASK ACTIVITY PROFILES
62
ACTIVITIES ESTIMATE
HW ARCH MODEL
64
60
α
• CACHES SIZES/ARCHITECTURES
• BUSSES WIDTH, I/O PIN NUMBERS
• WRITE BUFFERING, WRITE POLICY
• MEMORIES TYPES
• CLOCK SPEEDS
PROBABILISTIC VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME

FIG. 6

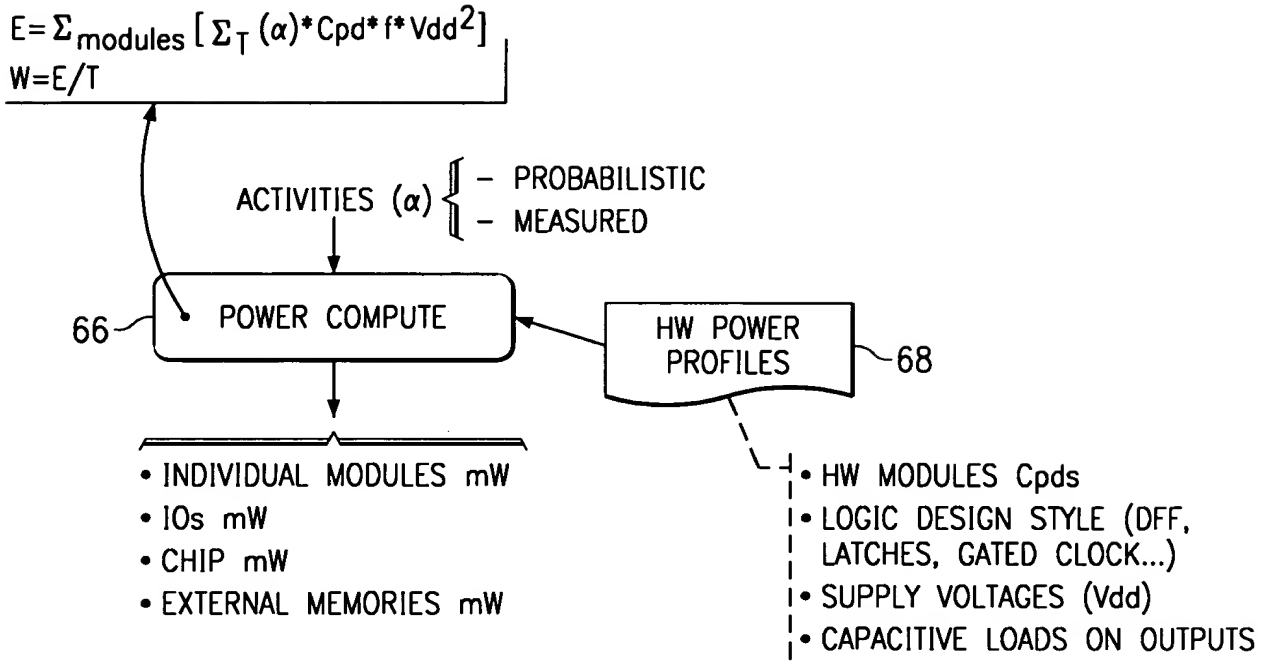
E=Σmodules [ΣT (α)*Cpd*f*Vdd2]
W=E/T
ACTIVITIES (α)
- PROBABILISTIC
- MEASURED
66
POWER COMPUTE
HW POWER PROFILES
68
• INDIVIDUAL MODULES mW
• IOs mW
• CHIP mW
• EXTERNAL MEMORIES mW
• HW MODULES Cpds
• LOGIC DESIGN STYLE (DFF, LATCHES, GATED CLOCK...)
• SUPPLY VOLTAGES (Vdd)
• CAPACITIVE LOADS ON OUTPUTS

FIG. 7

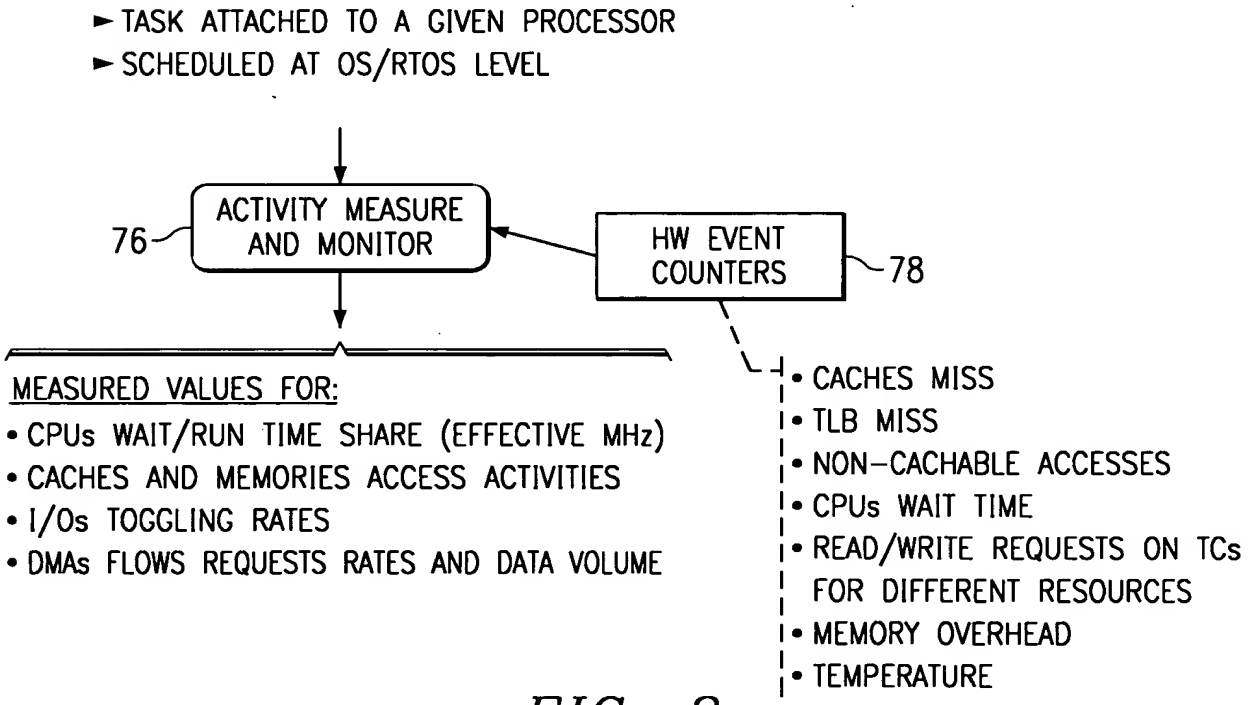
► TASK ATTACHED TO A GIVEN PROCESSOR
► SCHEDULED AT OS/RTOS LEVEL
76
ACTIVITY MEASURE AND MONITOR
HW EVENT COUNTERS
78
MEASURED VALUES FOR:
• CPUs WAIT/RUN TIME SHARE (EFFECTIVE MHz)
• CACHES AND MEMORIES ACCESS ACTIVITIES
• I/Os TOGGLING RATES
• DMAs FLOWS REQUESTS RATES AND DATA VOLUME
• CACHES MISS
• TLB MISS
• NON-CACHABLE ACCESSES
• CPUs WAIT TIME
• READ/WRITE REQUESTS ON TCs FOR DIFFERENT RESOURCES
• MEMORY OVERHEAD
• TEMPERATURE

FIG. 8

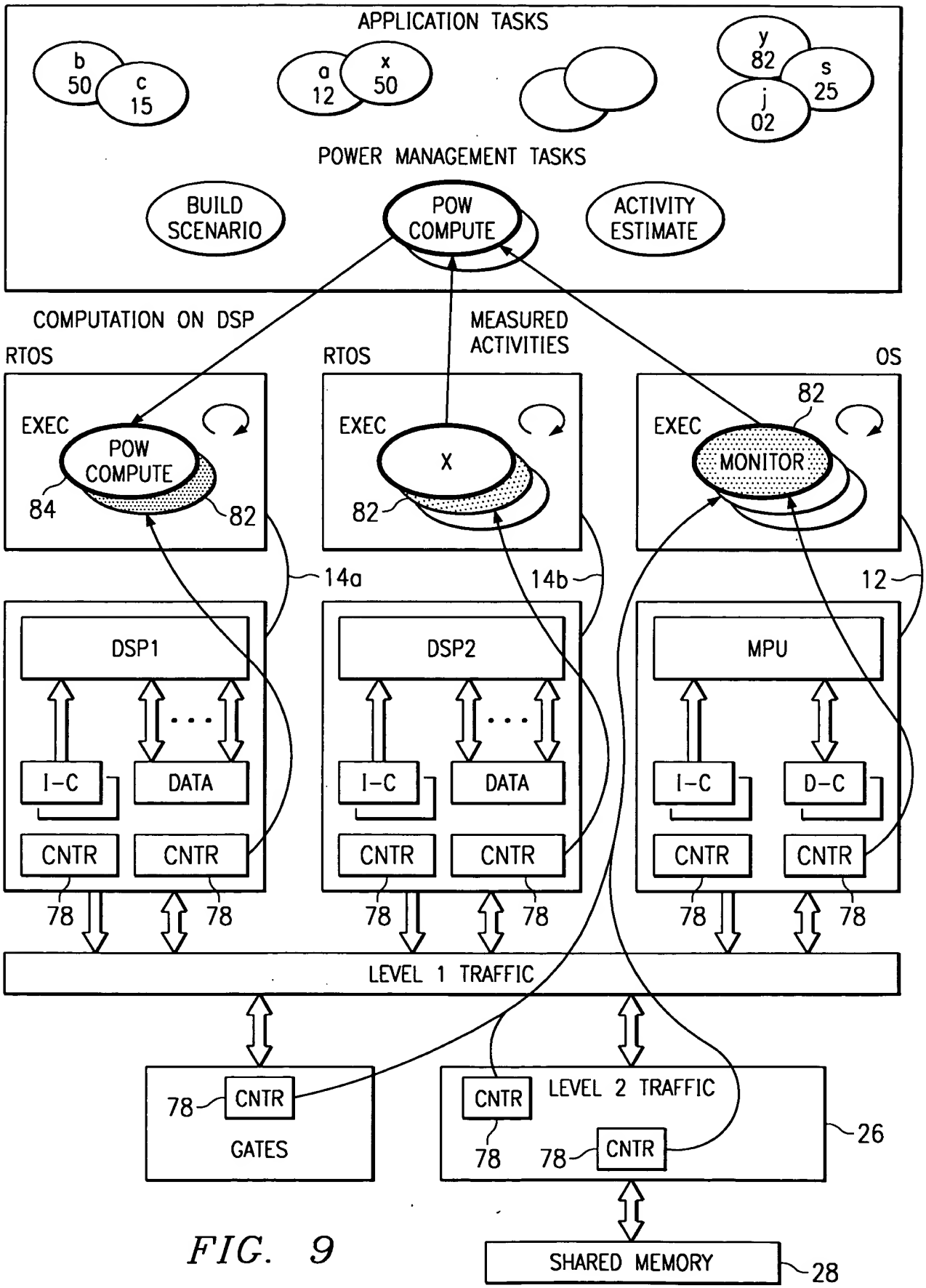
APPLICATION TASKS
b
50
c
15
a
12
x
50
y
82
s
25
j
02
POWER MANAGEMENT TASKS
BUILD SCENARIO
POW COMPUTE
ACTIVITY ESTIMATE
COMPUTATION ON DSP
MEASURED ACTIVITIES
RTOS
RTOS
OS
EXEC
POW COMPUTE
84
82
EXEC
X
82
EXEC
82
MONITOR
14a
14b
12
DSP1
DSP2
MPU
I-C
DATA
I-C
DATA
I-C
D-C
CNTR
CNTR
CNTR
CNTR
CNTR
CNTR
78
78
78
78
78
78
LEVEL 1 TRAFFIC
78
CNTR
GATES
CNTR
LEVEL 2 TRAFFIC
78
78
CNTR
26
SHARED MEMORY
28

FIG. 9

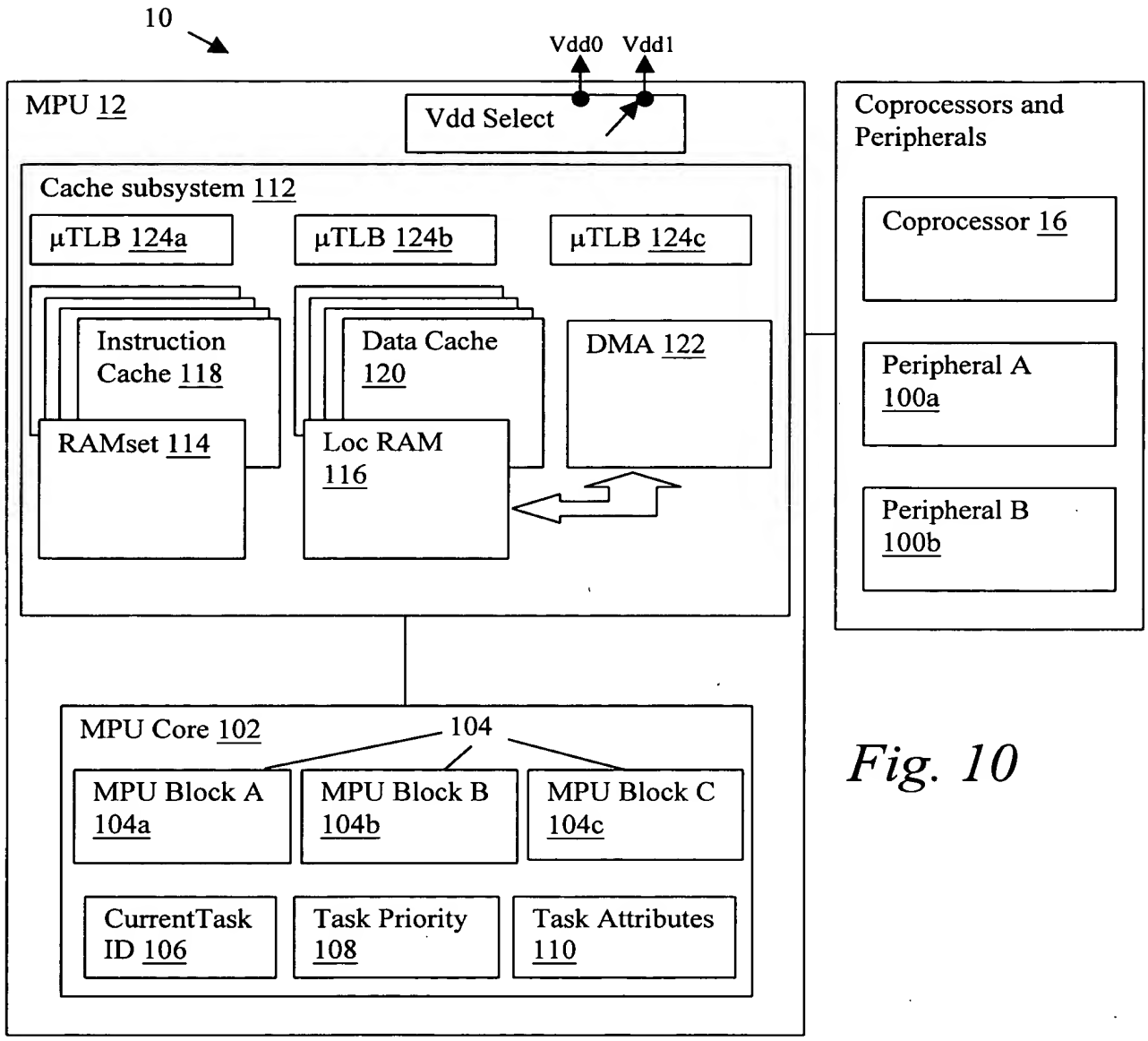
10
Vdd0
Vdd1
MPU 12
Vdd Select
Cache subsystem 112
µTLB 124a
µTLB 124b
µTLB 124c
Instruction Cache 118
Data Cache 120
DMA 122
RAMset 114
Loc RAM 116
MPU Core 102
104
MPU Block A 104a
MPU Block B 104b
MPU Block C 104c
CurrentTask ID 106
Task Priority 108
Task Attributes 110
Coprocessors and Peripherals
Coprocessor 16
Peripheral A 100a
Peripheral B 100b

Fig. 10

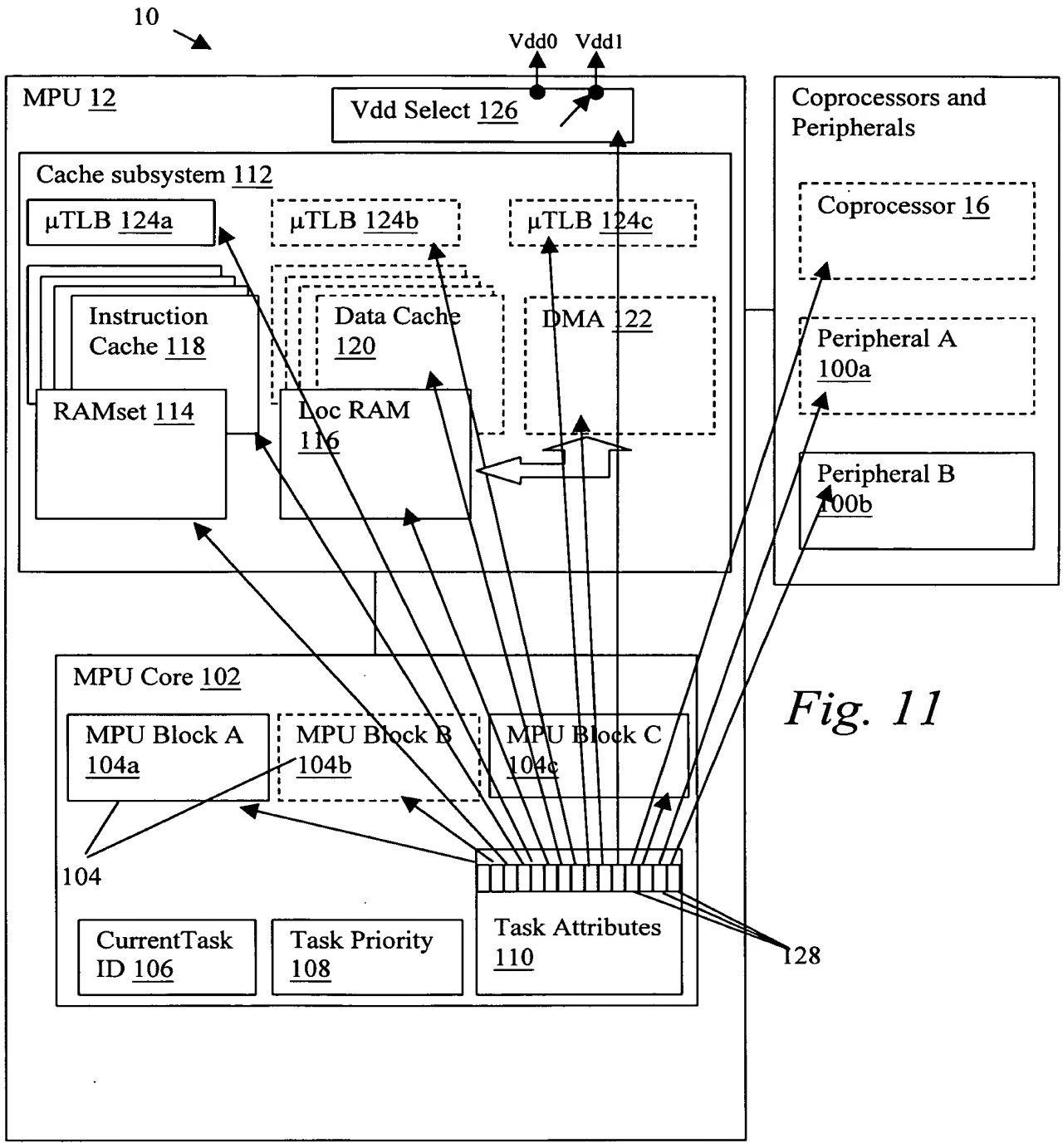
10
Vdd0
Vdd1
MPU 12
Vdd Select 126
Coprocessors and Peripherals
Cache subsystem 112
µTLB 124a
µTLB 124b
µTLB 124c
Coprocessor 16
Instruction Cache 118
Data Cache 120
DMA 122
Peripheral A 100a
RAMset 114
Loc RAM 116
Peripheral B 100b
MPU Core 102
MPU Block A 104a
MPU Block B 104b
MPU Block C 104c
104
CurrentTask ID 106
Task Priority 108
Task Attributes 110
128

Fig. 11

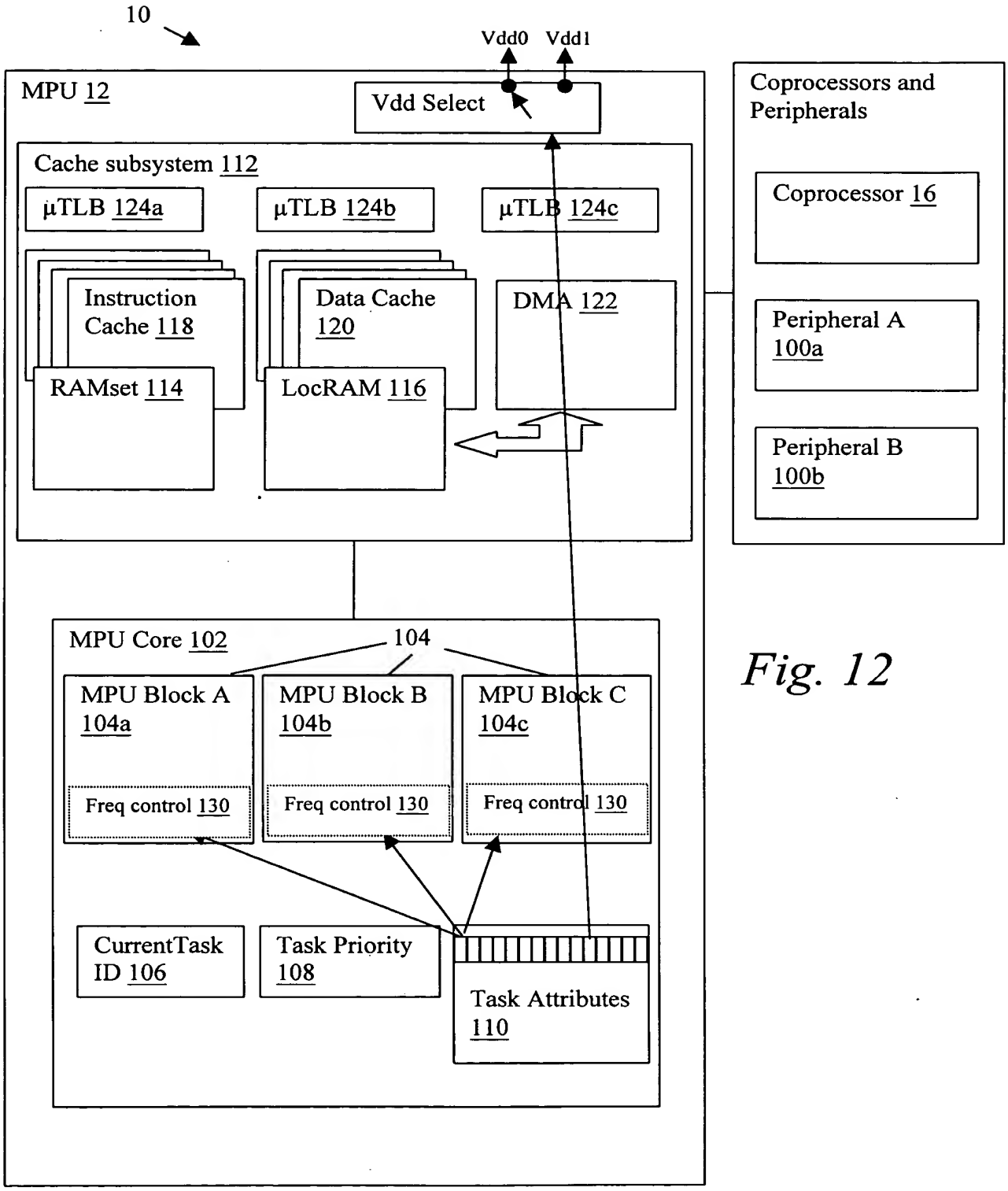
10
Vdd0
Vdd1
MPU 12
Vdd Select
Cache subsystem 112
µTLB 124a
µTLB 124b
µTLB 124c
Instruction Cache 118
RAMset 114
Data Cache 120
LocRAM 116
DMA 122
Coprocessors and Peripherals
Coprocessor 16
Peripheral A 100a
Peripheral B 100b
MPU Core 102
104
MPU Block A 104a
MPU Block B 104b
MPU Block C 104c
Freq control 130
Freq control 130
Freq control 130
CurrentTask ID 106
Task Priority 108
Task Attributes 110

Fig. 12

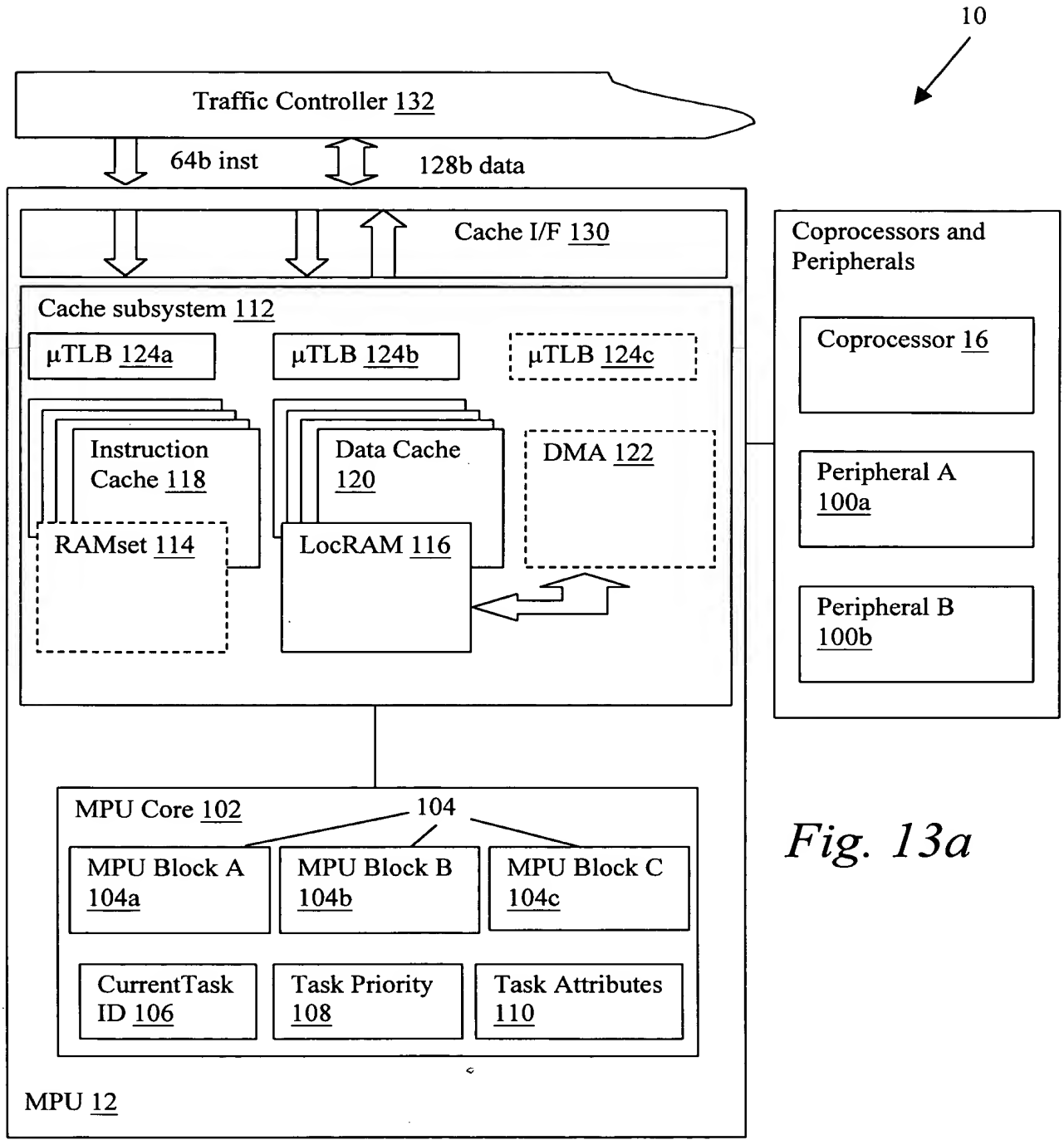
10
Traffic Controller 132
64b inst
128b data
Cache I/F 130
Cache subsystem 112
µTLB 124a
µTLB 124b
µTLB 124c
Instruction Cache 118
RAMset 114
Data Cache 120
LocRAM 116
DMA 122
Coprocessors and Peripherals
Coprocessor 16
Peripheral A 100a
Peripheral B 100b
MPU Core 102
104
MPU Block A 104a
MPU Block B 104b
MPU Block C 104c
CurrentTask ID 106
Task Priority 108
Task Attributes 110
MPU 12

Fig. 13a

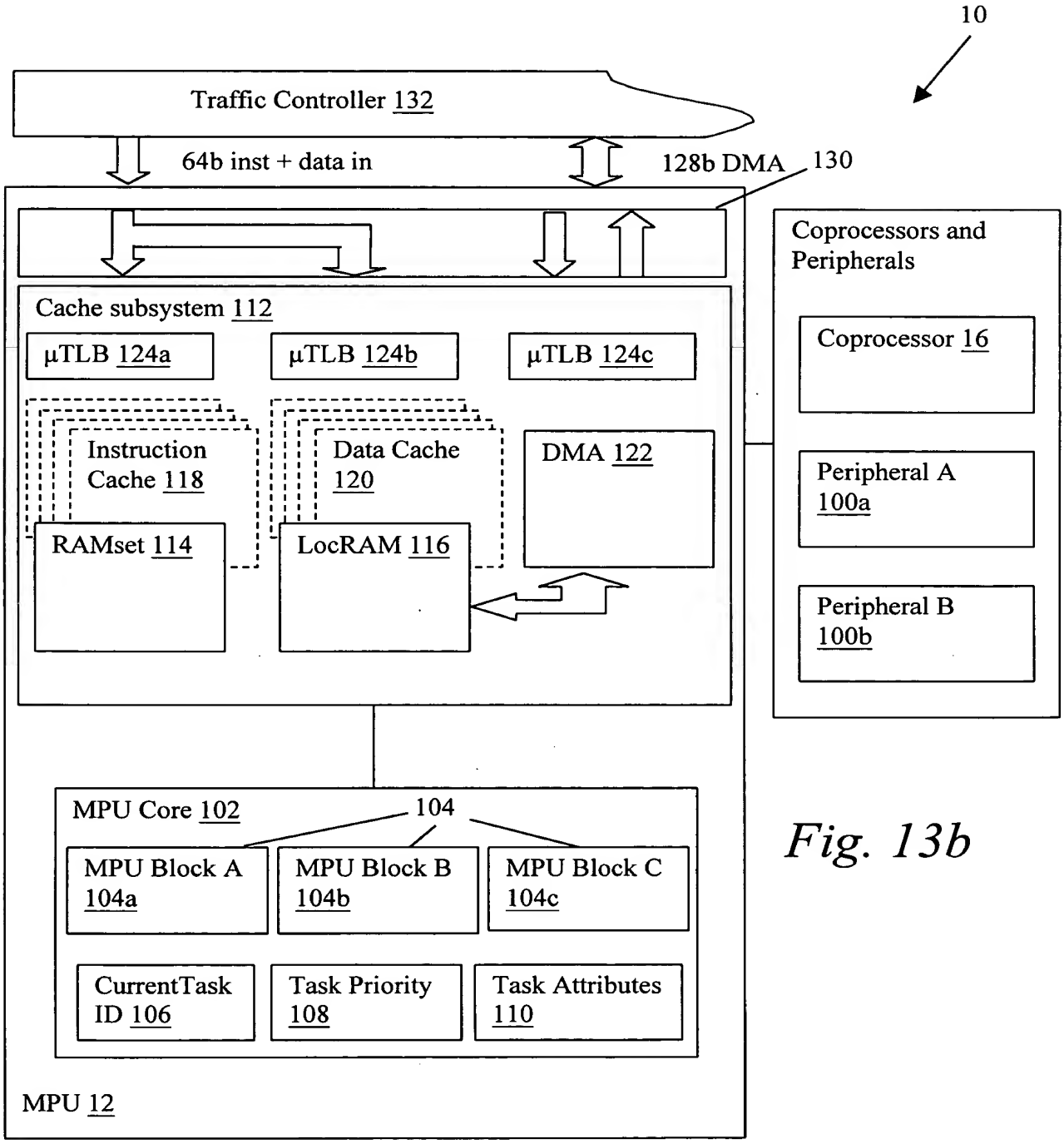
10
Traffic Controller 132
64b inst + data in
128b DMA
130
Coprocessors and Peripherals
Cache subsystem 112
µTLB 124a
µTLB 124b
µTLB 124c
Instruction Cache 118
Data Cache 120
DMA 122
RAMset 114
LocRAM 116
Coprocessor 16
Peripheral A 100a
Peripheral B 100b
MPU Core 102
104
MPU Block A 104a
MPU Block B 104b
MPU Block C 104c
CurrentTask ID 106
Task Priority 108
Task Attributes 110
MPU 12

Fig. 13b

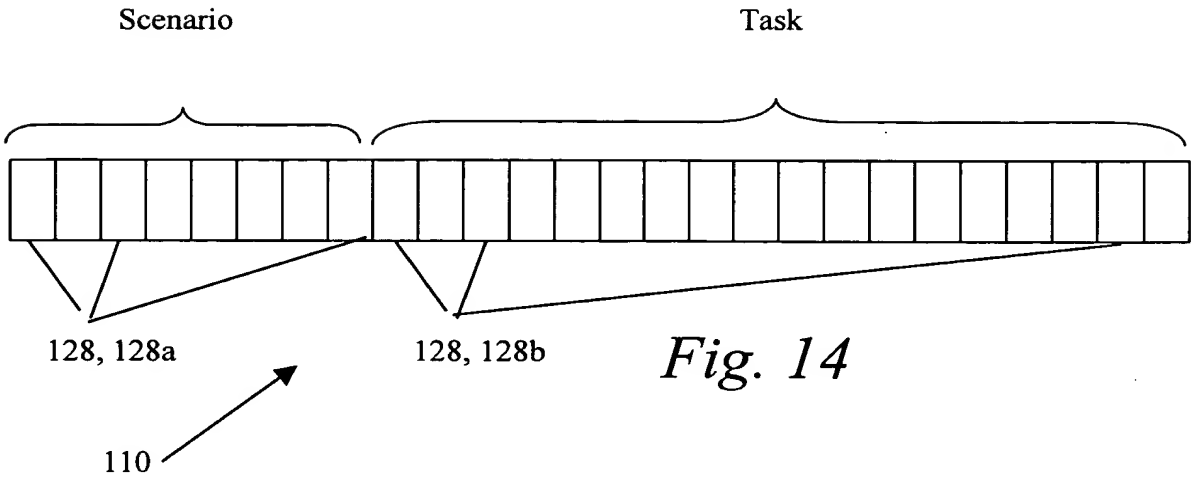
Scenario
Task
128, 128a
128, 128b
110

Fig. 14

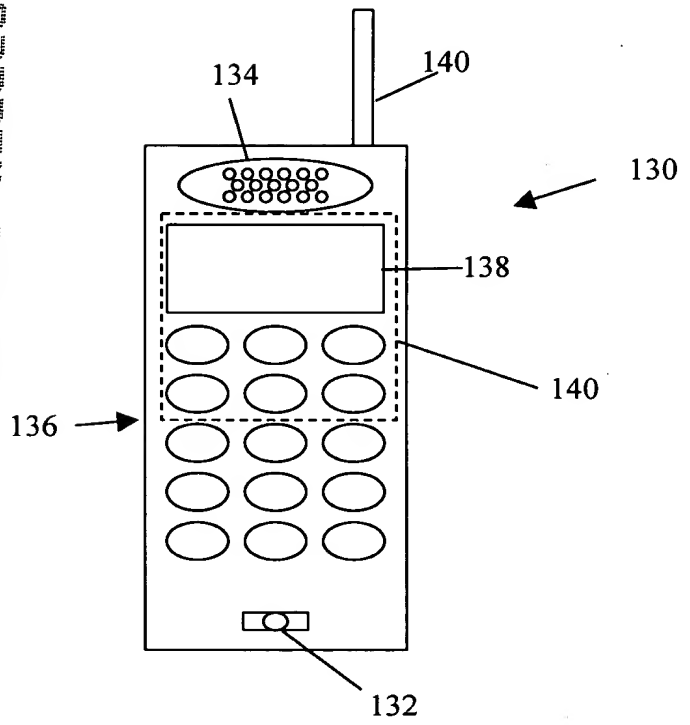
134
140
130
138
140
136
132

Fig. 16

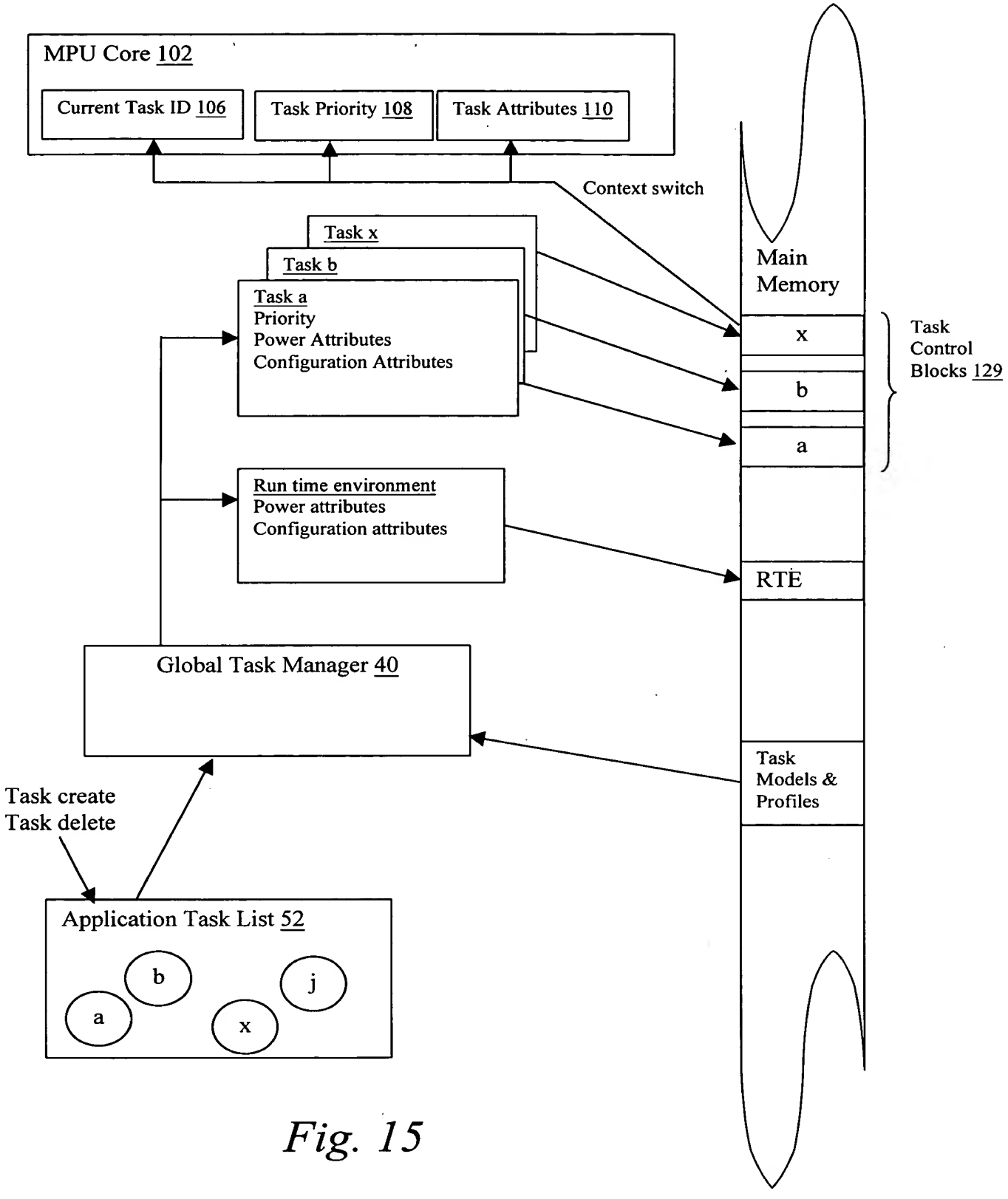
MPU Core 102
Current Task ID 106
Task Priority 108
Task Attributes 110
Context switch
Task x
Task b
Task a
Priority
Power Attributes
Configuration Attributes
Main Memory
x
b
a
Task Control Blocks 129
Run time environment
Power attributes
Configuration attributes
RTE
Global Task Manager 40
Task Models & Profiles
Task create
Task delete
Application Task List 52
b
j
a
x

Fig. 15